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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TOSHIHARU YANAGIDA

Appeal 2009-002327
Application 09/385,959
Technology Center 2800

Decided: December 31, 2009

Before KENNETH W. HAIRSTON, ELENI MANTIS MERCADER, and BRADLEY W. BAUMEISTER, *Administrative Patent Judges*.

MANTIS MERCADER, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant seeks our review under 35 U.S.C. § 134(a) of the Examiner's final rejection of claims 7, 8 and 10-21. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

INVENTION

Appellant's claimed invention is directed to providing a process of producing a semiconductor which enables the thermal stress between a semiconductor device and mounting board to be reliably relieved without the use of a sealing resin, reduces the connection resistance, and increases the strength of the joint portions (Spec. 9:10-16). The semiconductor having metal bumps formed so as to connect to a circuit pattern of a semiconductor device and a resin film formed on a circuit pattern forming surface of the semiconductor so as to seal spaces between the metal bumps and become thinner than the height of the metal bumps (Spec. 9:17-25). The metal bumps are solder bumps, and eutectic solder layers different in composition from the solder bumps are formed at the surfaces of the solder bumps projecting out from the resin film (Spec. 10:6-14).

Claim 7, reproduced below, is representative of the subject matter on appeal:

7. A method of producing a semiconductor apparatus, the method comprising the steps of:

forming metal ball bumps in direct contact with a circuit pattern of a semiconductor device formed on a semiconductor substrate in a semiconductor wafer state;

forming a resin film on a circuit pattern forming surface of said semiconductor device so as to seal spaces between said metal ball bumps and to become thinner than a height of the metal ball bumps;

cleaning the surfaces of the metal ball bumps projecting out from the resin film;

after the cleaning step, forming eutectic solder layers different in composition from the metal ball bumps on the surfaces of the metal ball bumps;

after the forming solder layers step, cutting the semiconductor substrate into unit semiconductor chips, each semiconductor chip having at least one of said semiconductor device;

and

after the cutting step, mounting at least one of the semiconductor chips on a mounting board from a bump forming surface side of the semiconductor chip so as to connect the eutectic solder layers of the semiconductor chip to the mounting board with the resin film directly contacting the semiconductor chip and not directly contacting the mounting board.

THE REJECTIONS

The Examiner relies upon the following as evidence of unpatentability:

Okumura	US 4,807,021	Feb. 21, 1989
Jackson	US 5,068,040	Nov. 26, 1991
Behun	US 5,147,084	Sep. 15, 1992

Hayes	US 6,114,187	Sep. 5, 2000 (Filed Jan. 8, 1998)
Denning	US 6,187,682 B1	Feb. 13, 2001 (Filed May 26, 1998)
Nishikawa	US 6,227,436 B1	May 8, 2001 (Filed Sep. 25, 1998)
Hotchkiss	US 2002/0106832 A1	Aug. 8, 2002 (Filed Nov. 5, 1997)

The following rejections are before us for review:

1. The Examiner rejected claims 7, 8, 10, 11, 16, and 19-21 under 35 U.S.C. § 103(a) as being unpatentable over Hayes in view of Hotchkiss and Behun.

2. The Examiner rejected claims 12, 13, and 17 under 35 U.S.C. § 103(a) as being unpatentable over Hayes in view of Hotchkiss and Behun and further in view of Nishikawa and Denning.

3. The Examiner rejected claims 14 and 15 under 35 U.S.C. § 103(a) as being unpatentable over Hayes in view of Hotchkiss, Behun, Nishikawa and Denning and further in view of Okumura.

4. The Examiner rejected claim 18 under 35 U.S.C. § 103(a) as being unpatentable over Hayes in view of Hotchkiss and Behun and further in view of Jackson.

Appellant argues rejected claims 7, 8, 10, 11, 16, and 19-21 as a group with claim 7 as the representative claim (App. Br. 4-6). Accordingly, claims 8, 10, 11, 16, and 19-21 stand or fall with claim 7. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUE

Appellant argues that Hayes teaches metal ball bumps 9 on top of solder columns 9 and dielectric layer 4, with no eutectic layers formed on its metal ball bumps 9 (App. Br. 4-5). Appellant further argues that Hayes' solder columns are not interchangeable with Hotchkiss's metal ball bumps because Hayes' express teaching of solder columns is to avoid accidentally short-circuiting its underlying electrical pads (citing Hayes, col. 9, l. 62-col. 10, l. 9), and as such, teaches away from using metal ball bumps (App. Br. 6). Appellant also argues that none of the combined references teaches or cures the stated deficiencies (App. Br. 6).

We note that Appellant minimally argues claims 12, 13-15, 17, and 18 (App. Br.7-9) reciting what the particular prior art references teach but with no attempt to point out how or why these claims patentably distinguish over the prior art, other than stating that they do not cure the above-cited deficiencies. Thus, Appellant's arguments do not amount to separate arguments for patentability. *See* 37 C.F.R. § 41.37(c)(1)(vii) (2004). *See also In re Nielson*, 816 F.2d 1567, 1572 (Fed. Cir. 1987). Thus, we only address the specific arguments presented.[1]

[1] Only arguments made by Appellant have been considered in this decision. Arguments which Appellant could have made but chose not to make in the Brief have not been considered and are deemed waived. See 37 C.F.R. § 41.37(c)(1)(vii) (2004).

Thus, Appellant's arguments present us with the following pivotal issue:

Has Appellant shown that the Examiner erred in finding that Hayes alone or in view of Hotchkiss teaches "forming metal ball bumps in direct contact with a circuit pattern of a semiconductor device" and "forming eutectic solder layers . . . on the surfaces of the metal ball bumps" as recited in claim 7?

FINDINGS OF FACT

The following findings of fact (FF) are supported by a preponderance of the evidence:

1. Hayes teaches that solder columns 3 are deposited or printed on the individual pads 2 of a chip 1, and solder balls 9 are deposited on top of columns 3 (Fig. 2e; col. 14-20).
2. Appellant does not contest that the columns are in direct contact with the circuit pattern (App. Br. 4).
3. Hayes (col. 10, ll. 18-30) teaches that "if the drops are very close together in time" (i.e., higher velocity), "they will solidify into one big ball of solder."
4. Hayes teaches that "[t]he effect of higher velocity is a tendency to spread the column a little more giving a fatter column" (col. 10, ll. 27-28).
5. Hayes teaches that "[i]f a longer time is provided between drops . . . tends to build a narrower taller column" (col. 10, ll. 20-23).
6. Hayes warns that the columns 3 should be placed far enough away from each other so that the overlaying solder balls 9 do not contact each other (col. 10, ll. 3-9).

7. Hotchkiss teaches (¶¶ [0033], [0036]), that cylindrical columns and solder balls can be alternatively used to be placed in direct contact with circuits in semiconductors.

PRINCIPLES OF LAW

The Examiner bears the initial burden of presenting a prima facie case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). If that burden is met, then the burden shifts to the Appellant to overcome the prima facie case with argument and/or evidence. *Id.*

The Examiner's articulated reasoning in the rejection must possess a rational underpinning to support the legal conclusion of obviousness. *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006). The Supreme Court, citing *In re Kahn*, 441 F.3d at 988, stated that "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). However, "the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *Id.*

"[O]ne cannot show non-obviousness by attacking references individually where . . . the rejections are based on combinations of references." *In re Keller*, 642 F.2d 413, 426 (CCPA 1981).

ANALYSIS

Rejection of claims 7, 8, 10, 11, 16, and 19-21

Hayes teaches that solder columns 3 are deposited or printed on the individual pads 2 of a chip 1 and solder balls 9 deposited on top of columns 3 (FF 1). Appellant does not contest that the columns are in direct contact with the circuit pattern (FF 2). The point of contention is whether Hayes teaches that these columns can be replaced with balls of solder or alternatively whether Hotchkiss teaches substitution of columns with metal balls as equivalent alternatives.

The Examiner takes the position (Ans. 3) that Hayes (FF 3) teaches that if the drops are too close together in time (i.e., higher velocity), they solidify into one big "ball of solder." We agree with Appellant's argument that this means that all the columns would become one "ball of solder" instead of individual columns (Reply Br. 4) because if all the columns are close to each other and the velocity of the drops increases all the columns will become one big ball. We note that while Hayes does teach that based on the velocity of the drops the columns can be "fatter" (FF 4) or "narrower" and taller (FF 5), Hayes does not explicitly state that the "fatter" columns can take the shape of balls.

However, we are not persuaded by Appellant's argument that Hayes (citing col. 9, l. 62-col. 10, l. 9) teaches that use of solder ball bumps instead of columns would accidentally short-circuit its underlying electrical pads (App. Br. 6). Hayes merely warns that the columns 3 should be placed far enough away from each other so that the overlaying solder balls 9 do not contact each other (FF 6). Nothing precludes columns 3 from being solder balls themselves as long as they

co-extend with the overlaying solder balls 9, and thus, far enough from each other. Furthermore, we agree with the Examiner (Ans. 5), that Hotchkiss teaches (FF 7), that cylindrical columns of solder and solder balls were art-recognized functionally equivalent alternative shapes for placing solder in direct contact with circuits in flip-chip semiconductors. Accordingly, Hayes' columns are replaceable by solder balls because Hotchkiss expressly provides this teaching.

For the foregoing reasons, we sustain the Examiner's rejections of claim 7 and claims 8, 10, 11, 16, and 19-21 which fall with claim 7.

Rejection of claims 12, 13-15, 17, and 18

Regarding the obviousness rejections of (1) claims 12, 13, and 17 over Hayes in view of Hotchkiss and Behun and further in view of Nishikawa and Denning, (2) claims 14 and 15 over Hayes in view of Hotchkiss, Behun, Nishikawa and Denning and further in view of Okumura and (3) claim 18 over Hayes in view of Hotchkiss and Behun and further in view of Jackson, we find that the Appellant has not persuasively rebutted the Examiner's prima facie case of obviousness for these claims, but merely contended that the additional references fail to cure the previously-noted deficiencies of Hayes with respect to claim 7 (App. Br. 7-9).

Once the Examiner has satisfied the burden of presenting a prima facie case of obviousness, the burden then shifts to Appellant to present evidence and/or arguments that persuasively rebut the Examiner's prima facie case. *See Oetiker*, 977 F.2d at 1445. Since Appellant did not particularly point out errors in the Examiner's reasoning to persuasively rebut the Examiner's prima facie case of obviousness, the rejections are therefore sustained.

CONCLUSION

Under 35 U.S.C. § 103, Appellant has not shown that the Examiner erred in finding that Hayes in view of Hotchkiss teaches "forming metal ball bumps in direct contact with a circuit pattern of a semiconductor device" and "forming eutectic solder layers . . . on the surfaces of the metal ball bumps."

ORDER

The decision of the Examiner to reject claims 7, 8 and 10-21 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

ELD

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